A PCB Packaging Platform Enabling 100+ Gbaud Optoelectronic Device Testing

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***Abstract*— We present a packaging platform that enables testing of co-packaged electronic and photonic integrated circuits and components, and that is based on a low-cost FR-4 PCB. The platform is capable of high speed electronic and optoelectronic transmitter and receiver assembly testing, and we demonstrate operation above 100 Gbaud.**

***Index Terms*— PCB, integrated optoelectronics, optical link**

I. INTRODUCTION

The demand for additional network bandwidth in data centers is ever-increasing. In order to meet transceiver datarate targets, designers of future generations of intra-datacenter optical interconnects will need to add additional optical lanes, use more spectrally efficient modulation formats, and increase optical baudrates. Increasing baudrates from 50 Gbaud to 100 Gbaud will require increased component bandwidths for both optical and electrical transceiver components, and careful transceiver packaging design to maintain radio frequency (RF) signal integrity, while at the same time maintaining good power efficiency and low cost.

A low-cost printed circuit board (PCB) packaging platform for testing optoelectronic devices beyond 100 Gbaud will be presented here. The platform is flexible, and can be used to test standalone transmitter and receiver electronic integrated circuits, as well as copackaged assemblies that include photonic integrated circuits or components. The platform is based on an FR-4 PCB with wirebonded connections for high speed signals on-chip, which lowers cost and assembly effort compared to more specialized PCB materials and flip-chip bonding alternatives. A similar PCB packaging platform has previously been used to demonstrate high baudrate [1] and high density [2] optical links. The platform presented here platform was used to perform the high speed measurements reported in [3]–[5]. The high baudrate testing enabled by this platform will be crucial for developing the high speed photonic and electronic integrated circuits (ICs) that will make possible future generations of optical interconnects, and it can also inform the design of the module packaging for 100+ Gbaud intra-datacenter transceivers.

Section II will present an overview of the various aspects of the PCB packaging platform. Section III will detail the design, optimization, and performance of the high speed signal path. High speed time-domain measurement results achieved using this packaging platform will be shown in Section IV. Finally, concluding remarks will be made in Section V.

II. PLATFORM OVERVIEW

This flexible platform can support packaging and testing of multiple different types and configurations of electronic ICs (EICs) and photonic ICs (PICs), and some representative example configurations will be shown. One example of a fully assembled PCB supporting a single channel high speed photoreceiver is shown in Fig. 1, with the locations of the IC, photonic components, and connectors highlighted.

A. High Speed Signals

In this platform, wirebonds are used to deliver high speed signals to and from the chips. Assemblies are carefully designed to limit RF wirebond length and thus maintain an acceptable amount of parasitic inductance. Fig. 2 shows closeup views of two wirebonded assemblies with electronic ICs copackaged with photonic components, in which the RF wirebonds at the tops and bottoms of the ICs are as made as short as possible given the assembly spacing constraints. For reference, the electronic ICs (EICs) in Fig. 2 are 1 mm $\times$ 1 mm.

Microstrip lines route the high speed signals across the PCB. Since FR-4 PCB material is used, the RF losses of the microstrip lines are dominated by the dielectric losses, and can be quite high. However, by minimizing the on-board microstrip trace length, these losses can be reduced so much that they no longer dominate the RF losses of the full packaging platform. In order to prevent crosstalk, the microstrip ground plane separates and isolates the RF microstrip traces, which are located in the top metal layer, from the other DC traces, which are routed in lower metal

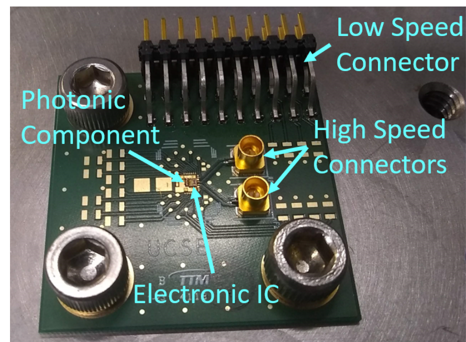

Fig. 1. An example optoelectronic assembly on an FR-4 PCB.

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layers. Vias also provide ground plane stitching around the RF traces to further reduce crosstalk and maintain signal integrity.

The high speed signals are brought on and off the PCB through Mini-SMP connectors (Rosenberger 18S102-40ML5). The design, optimization, and measurement showing a 60 GHz bandwidth of the connector and optimized on-board launch structure will be presented in detail in Section III. Once brought off the PCB, coaxial cables deliver the high speed signals to and from the test equipment. For high speed time domain testing, the coaxial cables introduce losses that cannot be calibrated out, making it crucial to minimize their lengths as well, ideally to $\leq$ 4in per cable. Carefully managing RF signal integrity in all of these parts of the PCB packaging platform is critical for enabling high baudrate testing.

B. Low Speed Signals

The power distribution and low-speed signalling capabilities of the package are also critical for high speed testing of electronic and photonic integrated circuits. In this platform, low speed signals, once bonded out of the EICs and PICs, are brought to a standard header for interfacing with a variety of test equipment. To the extent possible, supplies and DC signals are decoupled directly on electrical ICs with integrated capacitors. However, since on-chip decoupling is space limited and can be inadequate for critical supplies, surface mounted wirebondable capacitors are mounted directly adjacent to the device under test, as shown in Fig. 2. The close location of the decoupling capacitor to the IC is crucial to minimize parasitic wirebond inductance that would degrade noise performance. If required, larger surface mount capacitors can also be placed further away on the PCB to provide additional decoupling.

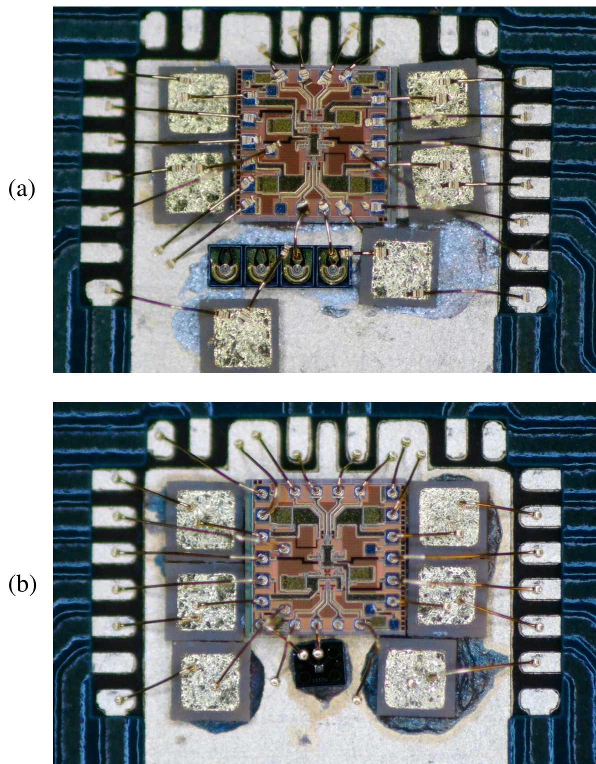

Fig. 2. Example optoelectronic assemblies, zoomed to show wirebonding detail. (a) Transmitter assembly including copackaged electronic driver IC, VCSEL array, and surface mount decoupling capacitors. (b) Receiver assembly including copackaged electronic TIA, vertically incident photodiode, and surface mount decoupling capacitors.

C. Optical Assembly

This packaging platform is compatible with a wide variety of optical devices for copackaging. Vertically incident optical devices, such as discrete photodiodes, vertical cavity surface emitting lasers (VCSELs), or vertically coupled PICs, can easily be packaged and fiber-coupled by aligning a fiber vertically above the chip. Edge coupled PICs are also supported, provided there is clearance for the fiber above the PCB. If this is not the case, special care needs to be taken to design for vertical shimming or milling of the PCB to provide clearance.

Fig. 3(a) shows an example receiver assembly including a coherent receiver PIC and a receiver IC. Another assembly with a driver IC and a coherent transmitter PIC containing a Mach-Zehnder modulator (MZM) is shown in Fig. 3(b). The PICs were fabricated in the GlobalFoundries 9WG silicon photonic process, and the EICs were fabricated in the GlobalFoundries 8XP process. In both of these assemblies, a section of the PCB under the PIC was milled away in order to match the chip height of the 250 μm thick EICs with the 750 μm thick PICs to within $\pm$50 μm. This is critical for minimizing the length of the EIC-to-PIC RF wirebonds, which are shown in detail in Fig. 3(c).

A critical consideration for maintaining the performance of many photonic devices, and especially integrated semiconductor diode lasers, is effective thermal management and heat sinking. In this platform, copper vias directly underneath the photonic and electronic ICs provide a low thermal impedance path for heat sinking. The PCB can also be mounted on a thermoelectric cooler (TEC) for further thermal management. In the case of the assemblies shown in Fig. 3, the thermally conductive epoxy and the copper thru-vias ensure that the PIC is well heat-sunk, even when the top metal layer has been milled away.

III. High Speed Design

The transition from the PCB microstrip line, to surface mounted Mini-SMP connector, to RF cable, is a critical point in the high speed signal path, and requires proper design to ensure minimal RF reflections and high bandwidth. Specifically, as noted in [2], the surface mounted RF connector creates additional capacitance at the PCB interface, causing the signal to no longer be in a 50 Ω environment. To counteract this effect, a portion of the ground plane directly below the RF connector was removed. Fig. 4 shows the simulation model of the connector launch structure geometry, with the ground plane cutout shown in black. The particular geometry of the launch structure with the removed ground plane was optimized in simulation using Ansys HFSS, and

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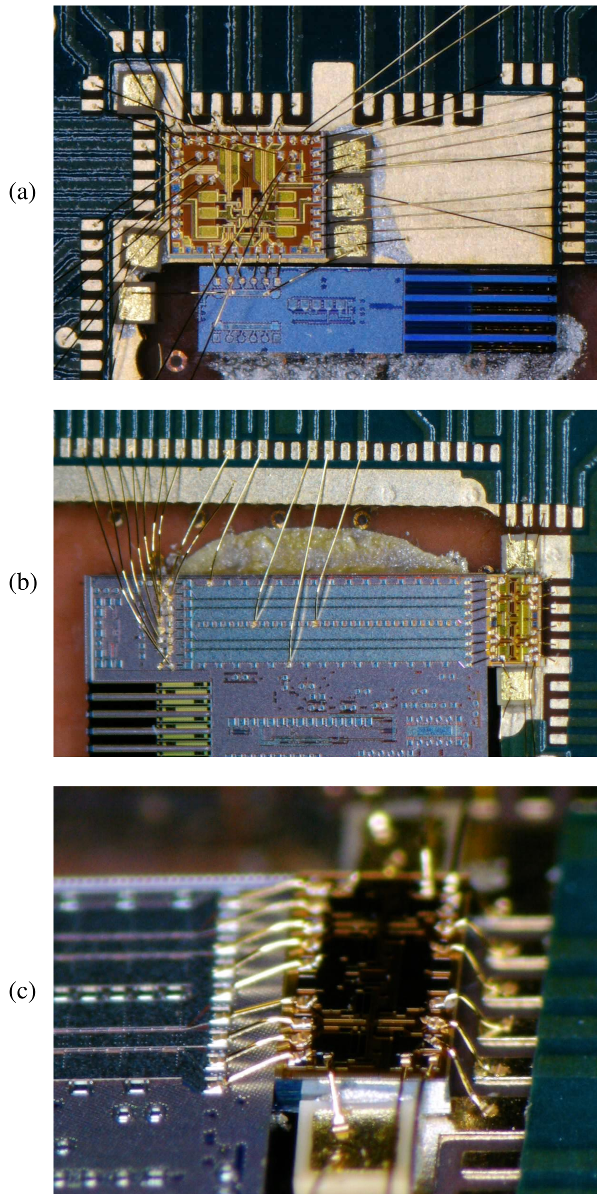

Fig. 3. Example optoelectronic assemblies, consisting of a silicon photonic receiver PIC with edge coupling copackaged with a receiver IC (a), and a driver IC copackaged with a silicon photonic transmitter PIC with edge coupling (b). The PCBs have been milled to accommodate different chip thicknesses. (c) A zoomed view of the transmitter assembly showing critical wirebonds between the EIC and PIC.

then further optimized by measuring the performance of various connector launch structures with skewed parameters.

The time domain reflectometry (TDR) impedance of the optimized second generation connector launch structure, measured with a 50 GHz TDR sampling module (Tektronix 80E10B), is shown in Fig. 5. The TDR measurement time can be mapped to physical distance in the device under test using the microwave index in each region, and thus the approximate locations of the PCB features have been labelled. The TDR impedance remains between 41 and 52 Ω throughout the entire connector launch structure. In addition

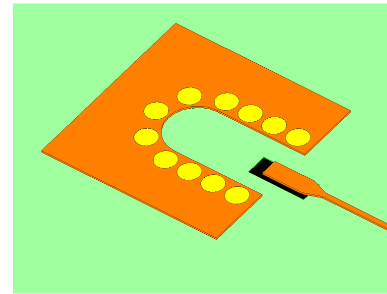

Fig. 4. The simulation model of the high speed connector launch structure, with the ground plane cutout shown in black.

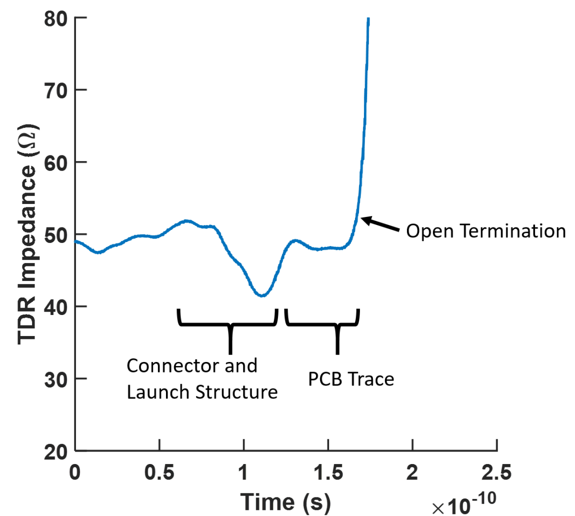

Fig. 5. Measured TDR Impedance for the high speed connector launch structure. Sections of the TDR trace are labelled with their corresponding physical structures.

to TDR characterization, simple microstrip structures with identical RF connector launch structures at both the input and output were also measured on a vector network analyzer (VNA). The extracted insertion loss and measured return loss of the optimized connector launch structure are shown in Fig. 6. The optimized structure has a 3 dB bandwidth of 60 GHz, as well as < 10 dB of return loss below 55 GHz.

The frequency dependent insertion loss of the PCB microstrip line and the RF coaxial cables were also extracted from the VNA measurements, and are shown, along with the connector launch structure loss and the calculated cascaded loss of a complete high speed path, in Fig. 7. Since low-cost FR-4 material was used for the PCB, the microstrip line can account for the highest RF losses in the entire packaging system if the traces are long. Thus, it is critical to minimize the length of the high speed traces on the PCB. For single differential input or differential output assemblies, such as the assembly in Fig. 1, we have reduced the microstrip length to just 5 mm, so that it no longer dominates the RF losses. Packaging chips that require large numbers of high speed traces requires careful design to keep trace lengths low and

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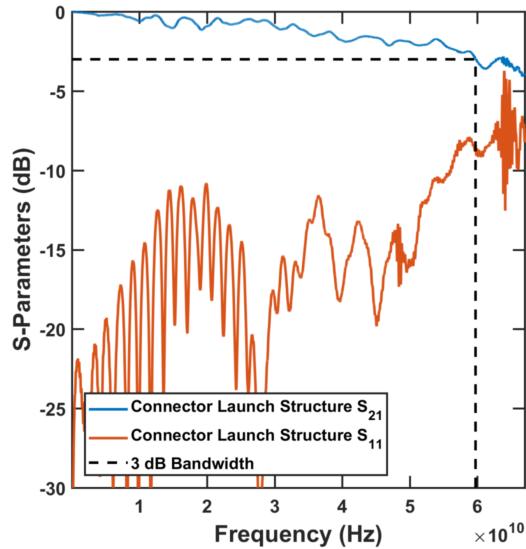

Fig. 6. Return loss and extracted insertion loss from S-parameter measurement of the fabricated high speed connector launch structure.

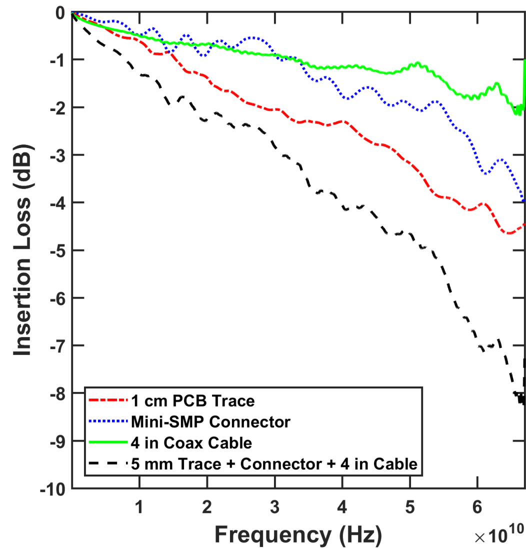

Fig. 7. Insertion losses extracted from S-parameter measurements for the PCB microstrip line, high speed connector launch structure, RF cables, and a cascaded high speed path. The curves have been smoothed to remove some measurement noise.

losses acceptable, and may eventually warrant a lower loss, albeit more expensive, PCB material choice.

IV. Experimental Demonstration

In this section, two demonstrations of high speed device and system measurement using this packaging platform will be shown. The first is a full optical link based on a vertical cavity surface emitting laser (VCSEL), which uses separate single channel transmitter and receiver PCB assemblies, and

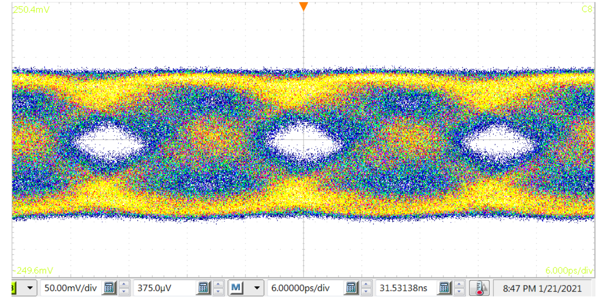

Fig. 8. Measured 50 Gbps electrical eye diagram at the receiver output for full VCSEL-based optical link operation using this packaging platform.

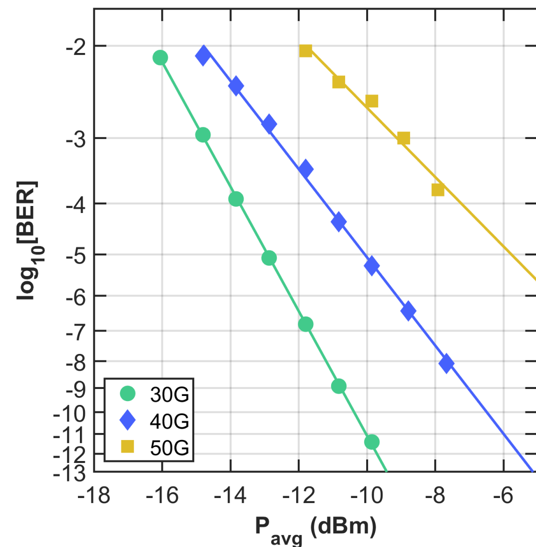

Fig. 9. Measured bit error rate vs average optical received power (assuming infinite extinction ratio) for the full VCSEL-based optical link operating at 30, 40, and 50 Gbps

the second is an all-electrical measurement of a packaged transimpedance amplifier (TIA).

A. Optical Link Characterization

The packaged transmitter and receiver assemblies shown in Fig. 2(a) and Fig. 2(b), respectively, were used to operate a full VCSEL-based optical link. The TIA circuit that was used is described in [5]. The link was characterized with a bit pattern generator (SHF 12104A) at the Tx input, and a digital sampling oscilloscope (Tektronix DSA8300) with a 70 GHz sampling module (Tektronix 80E11) at the Rx output. Fig. 8 shows the measured 50 Gbps non-return-to-zero (NRZ) eye at the Rx output for full link operation. Bit error rate (BER) sensitivity curves were measured with a bit error rate tester (BERT) (SHF 11104A) at the Rx output, and are shown in Fig. 9.

This result includes all of the bandwidth limitations from a cascade of the two separate Tx and Rx PCBs, including the wirebonds, microstrip lines, connectors, cables, driver and receiver circuits, and the VCSEL and photodiode. Notably, the VCSEL bandwidth on its own is 26 GHz. Despite these

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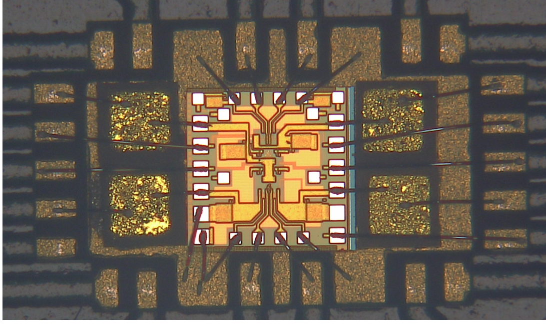

Fig. 10. Fully electrical TIA assembly.

limitations, an open eye was measured at 50 Gbps. Additionally, there is no indication of a BER floor at 50 Gbps, meaning that the amount of received optical power, not just the available bandwidth was limiting the link performance.

B. Electrical TIA Characterization

The same TIA chip used in the above optical link was also characterized in an electrical input and electrical output environment using this packaging platform. The packaged device is shown in Fig. 10. The time domain characterization was carried out with the same bit pattern generator and sampling oscilloscope module as above, but with the addition of a multiplexer (SHF 603A) at the Tx input to allow for NRZ signal generation above 64 Gbps. For BER measurements, a demultiplexer (SHF 623A) was inserted at the Rx output before the BERT. Electrical eye diagrams showing open eyes from 60 to 108 Gbps measured through the packaged device are shown in Fig. 11. Measurements showing BER $< 10^{-11}$ though this assembly were collected up to 96 Gbps. Higher datarate BER measurements were limited by the test setup clock distribution. More details of this measurement are presented in [5].

This measurement demonstrates that this FR-4 PCB packaging platform is capable of supporting device testing at speeds > 100 Gbaud. Since this chip is targeted for links with either either NRZ or quadrature phase shift keying (QPSK) modulation with an optical phase-locked loop (OPLL), as described in [6], the receiver chain has variable gain amplifier stages that limit the signal at high gain setting and effectively make a bit decision directly on chip. In cases like this, the EIC output stage can incorporate equalization that is designed to compensate for RF losses in the packaging and testing environment. For this TIA, a continuous-time linear equalizer (CTLE) circuit was included in the output stage. The equalized TIA output has 4 dB of peaking at 40 GHz, which helps to compensate for the expected packaging losses that were shown in Fig. 7. The CTLE has a relatively small impact on the overall device efficiency. The full TIA power efficiency was 1.5 pJ/bit, of which 0.3 pJ/bit is used in the output stage.

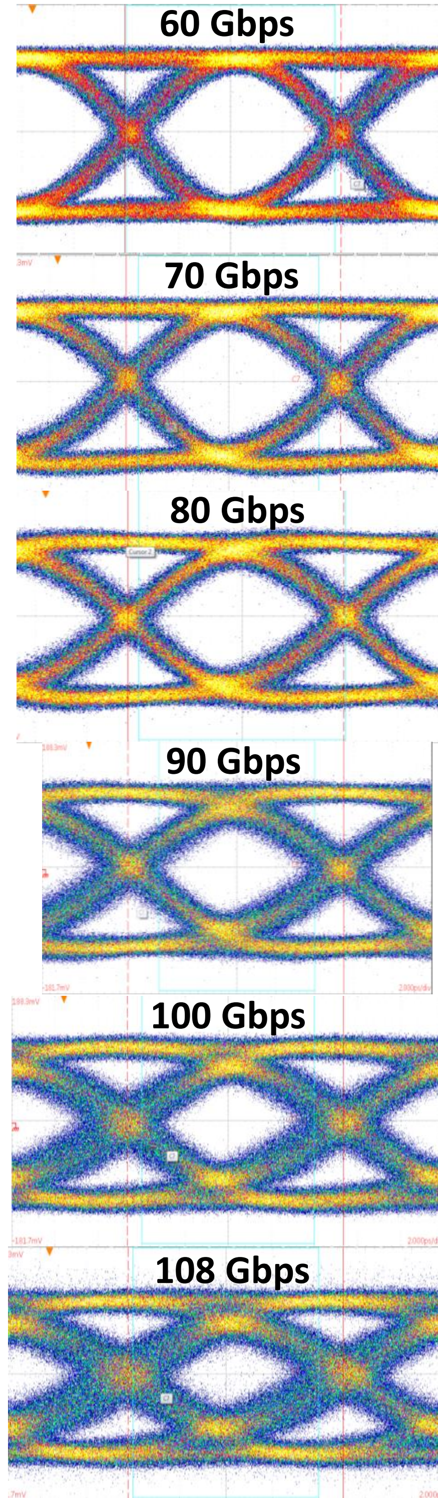

Fig. 11. Measured single-ended eye diagrams from 60 to 108 Gbps for the fully electrical TIA assembly.

V. Conclusion

An FR-4 PCB packaging platform for testing of copackaged optoelectronic devices at speeds up to and beyond

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100 Gbaud has been presented. Design and optimization of the RF performance of the various parts of the packaging system, and crucially the RF traces and high speed connector launch structure, was also described. This PCB packaging platform enables high baudrate testing that will be crucial for designing future generations of optical interconnects, and could also inform the packaging design for high baudrate, low cost intra-datacenter optical transceivers.

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