50 GBaud QPSK 0.98 pJ/bit Receiver in 45 nm CMOS and 90 nm Silicon Photonics

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Abstract *Low-power O-band receivers are required for next-generation coherent intra-datacenter interconnects. In this paper, a 0.98 pJ/bit QPSK receiver using a 45 nm CMOS process and a 90 nm Silicon Photonics (SiP) process is demonstrated at up to 50 GBaud.*

Introduction

Traffic within data centers is growing at over 23% per year[1]. As a result, there is increasing demand for scalable power-efficient intra-datacenter links. O-band coherent detection has important benefits for use in <2km optical interconnects. Coherent detection results in higher link margin than the intensity-modulation direct-detection (IM-DD) schemes in use today. This increase in link margin allows for more power efficient network architectures, such as those that utilize optical switching[2]. A key advantage of O-band is that the chromatic dispersion minimum of commercial single-mode fiber is located near 1310 nm, which relaxes DSP requirements.

The energy efficiency of coherent links to be used within the data center will depend heavily on the receiver electronics. Recently, a 56 GBaud monolithic O-band SiGe BiCMOS receiver with a power consumption of 485 mW has been reported[3]. Other relevant work includes a 34 GBaud DP-QPSK receiver consisting of a SiGe BiCMOS EIC and a SiP PIC with a power consumption of 313 mW per channel[4]. It has been estimated that the front-end transimpedance amplifier (TIA) and limiting amplifiers (LA) implemented in a SiGe BiCMOS, with an assumed combined power consumption of 410 mW, account for >40% of the total power in analog coherent intra-datacenter links that employ silicon photonics. This figure increases to >50% when indium-phosphide optics are utilized[5]. CMOS-based receiver electronics consume significantly less power than those implemented in SiGe BiCMOS, and thus can be a suitable alternative. The recent release of the GlobalFoundries (GF) 45CLO fabrication process demonstrates an industry trend towards monolithic integration of silicon photonics devices with CMOS transistors targeting low-cost, mass-production, and high performance optical transceivers[6], for which low-power receiver topologies will be required.

In this paper, we present a single-polarization O-band QPSK receiver consisting of an electronic integrated circuit (EIC) fabricated in the GF 45RF-SOI 45 nm CMOS process and a photonic integrated circuit (PIC) fabricated in the GF 9WG process. Experimental results demonstrate the operation of the receiver at up to 50 GBaud.

Receiver design

Fig. 1 shows a block diagram of an optical QPSK Costas loop receiver designed for analog coherent intra-datacenter links[2]. The focus of this paper, denoted by the dashed area, is the design and characterization of the electronics in the QPSK data signal path and their integration with the PIC.

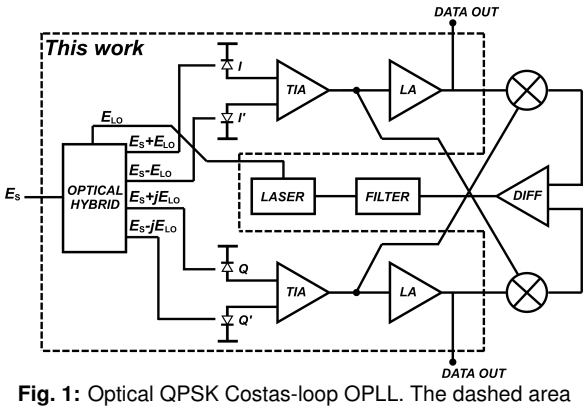

Fig. 1: Optical QPSK Costas-loop OPLL. The dashed area denotes the work presented in this paper.

A block diagram of the PIC and the EIC is shown in Fig. 2. The optical hybrid receives a CW laser signal (E_{LO}) and a QPSK modulated signal (E_S) and generates the four signals corresponding to the desired vectorial additions of the two input optical fields, which are routed to two pairs of balanced photodiodes (PD), one for the in-phase

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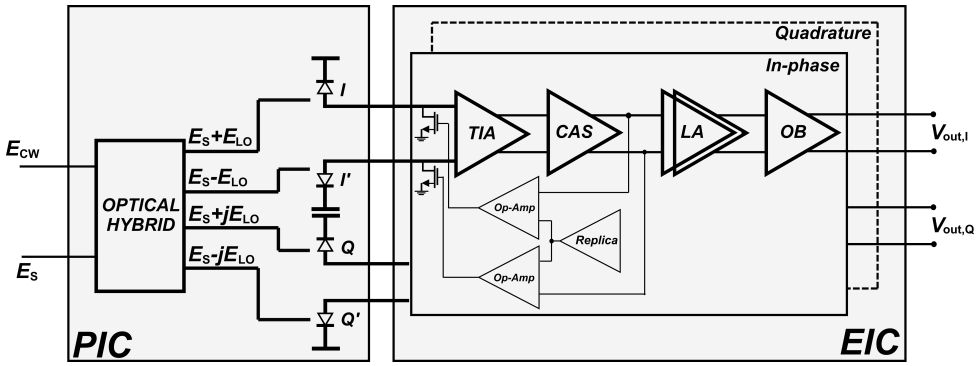

Fig. 2: Optical receiver block diagram. The PIC consists of an optical hybrid and 4 photodiodes. The photodiode anodes are connected via wirebonds to the TIA inputs of the EIC.

(I) channel and the other for the quadrature channel (Q). The electronics consist of a TIA, a cascode amplifier (CAS), a cascade of LAs, and an output buffer (OB). A slow loop based on a replica TIA and Op-Amps is used for DC-offset compensation (DCOC) and to sink any excess DC photocurrent.

Fig. 3 shows the schematic of the receiver TIA and cascode amplifiers. Connected to each PD there is an inverter shunt-feedback TIA. The inverter topology combines both NMOS and PMOS transconductances, resulting in high gain at low power consumption[7][8] and the pseudodifferential configuration saves power by minimizing the voltage headroom. At the TIA output, a cascode amplifier is used to raise the common-mode voltage to the required value for the subsequent source-coupled limiting amplifiers.

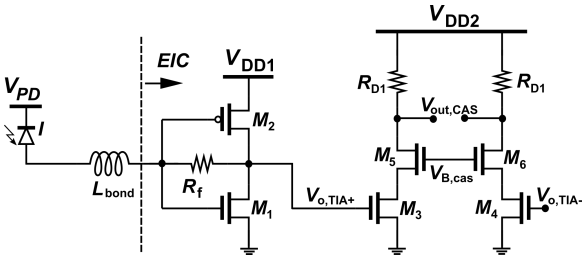

Fig. 3: Schematic of the receiver TIA and cascode amplifiers.

Source-coupled amplifiers were utilized for the LA and OB stages to provide common-mode rejection. The LA chain consists of six cascaded amplifiers of increasing transistor widths to minimize the loading between stages. The schematic of the LA and OB stages, depicted in Fig. 4, shows only one of the LA stages. R_S and varactor C_S provide tunable equalization. The 50 Ω OB has shunt inductive peaking to compensate for the output channel loss.

The simulated post-layout 3 dB BW assuming a 40 GHz PD BW, and including wirebonds and bondpad capacitances, is 23 GHz. The simulated midband transimpedance is 55 dBΩ.

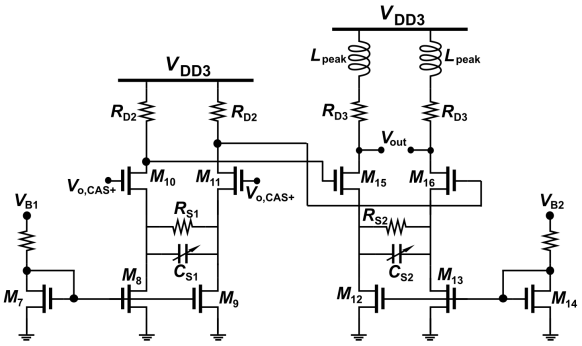

Fig. 4: Schematic of the source-coupled limiting amplifiers and output buffer.

Experimental results

The measured power consumption of the EIC including the OB is 98 mW, or 0.98 pJ/bit for 50 GBaud QPSK transmission. If the OB is omitted, in case a 50 Ω output is not required, the power is reduced to 77 mW, or 0.77 pJ/bit. The measured output noise of the EIC is 3 mV rms, the midband transimpedance is 477 Ω, and the calculated input-referred noise is 6.3 μA rms.

Fig. 5 shows the receiver assembly on a PCB. The EIC dimensions are 1.88 mm x 1.28 mm and the PIC dimensions are 6 mm x 1.1 mm. The PIC-to-EIC and EIC-to-PCB wirebonds are approximately 200 μm and 750 μm, respectively. Off-chip 1.2 nF bypassing capacitors were added to the PD and EIC supplies. Mini SMP RF connectors are used to measure the two differential data outputs.

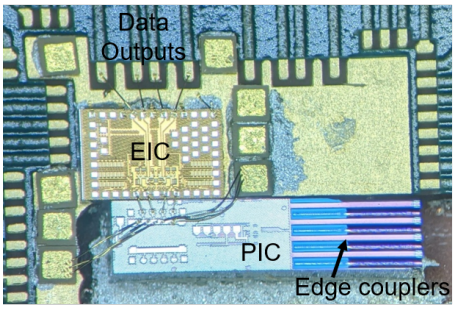

Fig. 5: Receiver assembly on a PCB.

Fig. 6 shows the self-homodyne test setup

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used. An EXFO T100S-HP-O external cavity laser (ECL) set to 1310 nm and 13 dBm of power is connected to a 3 dB coupler. One coupler output is connected to an iXblue MXIQER-LN-30 IQ-MZM. Two channels of an SHF 12104A BPG are amplified and used to drive the IQ-MZM to generate the QPSK signal, which is then amplified using a praseodymium-doped fiber amplifier (PDFA) and edge-coupled to the PIC. The other output of the 3 dB coupler is amplified using a semiconductor optical amplifier (SOA) and then connected to an attenuator, the output of which is edge-coupled to the PIC. The EIC outputs are connected to a Keysight real-time oscilloscope (RTO) and the samples are compared to the PRBS sequence for error counting. The specified BW of the IQ-MZM is 25 GHz. To compensate for the IQ-MZM response, feed-forward equalization (FFE) was constructed using two outputs of the BPG with a coaxial power combiner.

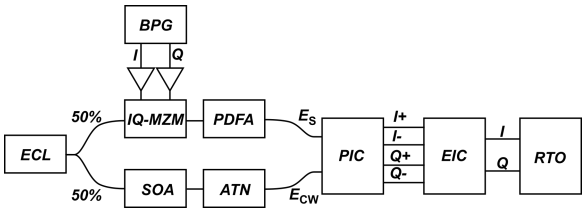

Fig. 6: QPSK self-homodyne measurement test setup. Polarization controllers and length-matching fiber are omitted from the schematic.

The PD responsivity is assumed to be 1 A/W. The data was taken at equal E_{CW} and E_S powers to minimize the DC current and thus minimize the shot noise for a given PD current swing. This way the receiver is characterized in terms of the circuit input-referred noise sensitivity and the inter-symbol interference (ISI) power penalty. At a high E_{CW} power, for instance for 0 dBm received power at each PD, the shot noise for a 40 GHz PD BW is 3.6 μA rms, which added to the measured circuit input-referred noise results in an approximate power penalty of 2.4 dB when operating near the HD-FEC limit. The measurements are expressed in terms of OMA received at each PD. All constellations consist of at least 2^{18} points and were generated using PRBS15. Measured constellations at 40 GBaud with OMA of -7.6 dBm and 50 GBaud with OMA of -5.5 dBm are shown in Fig. 7a and 7b, respectively. At 40 GBaud the FFE tap/main ratio was set to 0.5 and at 50 GBaud the ratio was set to 0.65. At 40 GBaud the BER is 1.2 x 10^{-5} and at 50 GBaud the BER is 9.7 x 10^{-4}, which is below the hard-decision forward error-correction (HD-FEC) limit of 3.8 x 10^{-3}.

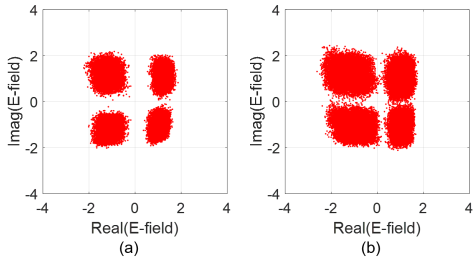

Fig. 7: Measured QPSK constellations at (a) 40 GBaud and (b) 50 GBaud, both with FFE applied to the IQ-MZI. The measured voltage swings are 60 mVpp and 80 mVpp for 40 GBaud and 50 GBaud,respectively.

The measured BER for various data rates, with and without transmitter FFE, is plotted versus OMA in Fig. 8. At 50 GBaud with FFE, the BER is below the HD-FEC limit for an OMA of -8.4 dBm. At 40 GBaud without FFE the OMA is -8.7 dBm.

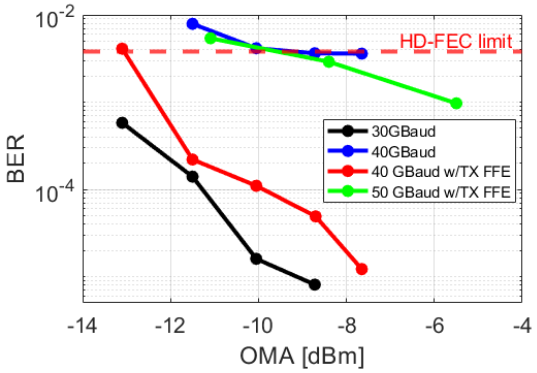

Fig. 8: BER vs. OMA received at each PD

Conclusions

In this work, we presented a 0.98 pJ/bit single-polarization O-band QPSK receiver fabricated in 45 nm CMOS and a 90 nm SiP process. The operation of the receiver was demonstrated at up to 50 GBaud below the HD-FEC BER limit. With these results, we believe that the PIC and the electronics can be utilized within a carrier recovery system such as QPSK costas loop to enable low power intra-datacenter optical links.

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